CLAIMS

What is Claimed is:

1. A microelectronic structure comprising:

a semi-conducting substrate comprising circuits therein and a top surface; and

at least one first conductive bump situated on said top surface providing electrical communication to said circuits, said at least one conductive bump having a sidewall formed of an electrically insulating material.

2. A microelectronic structure according to claim 1, wherein said sidewall formed of an electrically insulating material at least partially covers a periphery of said at least one first conductive bump.

3. A microelectronic structure according to claim 1, wherein said sidewall formed of an electrically insulating material covers completely a periphery of said at least one first conductive bump while leaving a top surface of said at least one first conductive bump exposed.

4. A microelectronic structure according to claim 1, wherein said sidewall formed of an electrically insulating material at least covers a section of said sidewall in said periphery of said at least one first conductive bump that is juxtaposed to a second conductive bump situated immediately adjacent to said at least one first conductive bump.

5. A microelectronic structure according to claim 1, wherein said electrically insulating material comprises organic material and inorganic material.

6. A microelectronic structure according to claim 1, wherein said electrically insulating material comprises a photosensitive material.

7. A microelectronic structure according to claim 1, wherein said at least one first conductive bump is formed of a conductive metal selected from the group consisting of Au, Ag, Pt, Pd, Al, Cu, Sn and alloys thereof.

8. A microelectronic structure according to claim 1, wherein said at least one first conductive bump having a height between about 5 μm and about 50 μm.

9. A microelectronic assembly comprising:

a semi-conducting substrate having at least one conductive bump situated on a top surface, said at least one conductive bump having a sidewall formed of an electrically insulating material;

an electronic substrate having at least one conductive pad situated on a top surface; and

an anisotropic conductive film sandwiched in-between said semi-conducting substrate and said electronic substrate, said anisotropic conductive film comprising at least one electrically conductive particle providing electrical communication between said at least one conductive bump and said at least one conductive pad.

10. A microelectronic assembly according to claim 9, wherein said semi-conducting substrate is an integrated circuit chip and said electronic substrate is a printed circuit board or a glass substrate.

11. A microelectronic assembly according to claim 9, wherein said sidewall formed of an electrically insulating material at least partially covers a periphery of said at least one conductive bump.

12. A microelectronic assembly according to claim 9, wherein said sidewall formed of an electrically insulating material covers completely a periphery of said at least one conductive bump while leaving a top surface of said at least one conductive bump exposed.

13. A microelectronic assembly according to claim 9, wherein said at least one conductive bump is formed of a conductive metal selected from the group consisting of Au, Ag, Pt, Pd, Al, Cu, Sn and alloys thereof.

14. A method for fabricating a microelectronic structure comprising the sequential steps of:

providing a semi-conducting substrate comprising circuits therein;

forming at least one first conductive bump on a top surface of said semi-conducting substrate;

conformally depositing a layer of insulating material on said at least one first conductive bump and said top surface of the semi-conducting substrate; and

removing selectively said layer of insulating material from a top surface of said at least one first conductive bump while leaving a sidewall of said at least one first conductive bump covered by said layer of insulating material.

15. A method for fabricating a microelectronic structure according to claim 14, wherein said removing step is carried out by a method selected from the group consisting of polishing, dry etching and lithography.

16. A method for fabricating a microelectronic structure according to claim 14, wherein said removing step is carried out by chemical mechanical polishing.

17. A method for fabricating a microelectronic structure according to claim 14 further comprising the step of forming said at least one first conductive bump to a height between about 5 μm and about 50 μm.

18. A method for fabricating a microelectronic structure according to claim 14 further comprising the step of forming said at least one first conductive bump from a material selected from the group consisting of Au, Ag, Pt, Pd, Al, Cu, Sn and alloys thereof.

19. A method for fabricating a microelectronic structure according to claim 14 further comprising the step of depositing conformally said layer of insulating material selected from the group consisting of organic materials and inorganic materials.

20. A method for fabricating a microelectronic structure comprising the sequential steps of:

providing a semi-conducting substrate comprising circuits therein;

forming at least one bump of a photosensitive material on a bond pad situated on said semi-conducting substrate, said photosensitive material is electrically insulating;

patterning and developing said at least one bump such that only a sidewall remaining after said developing process; and

filling a cavity formed by said sidewall by electroplating and forming at least one electrically conductive bump surrounded by said electrically insulating photosensitive material on its peripheral surface, said at least one electrically conductive bump in electrical communication with said circuits in said semi-conducting substrate.